

REMARKS

Prior to entry of the present Amendment, claims 1-21 were pending in the present application. Claim 1 is amended above. Claim 20 is cancelled above. No new matter is added by the claim amendments. Entry is respectfully requested.

The Applicants note, with appreciation, that the Office Action dated June 20, 2006 indicates, at page 6, section 8, that claims 10-18 and 21 are allowed.

Claims 19 and 20 stand rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Claim 20 is cancelled above.

With regard to claim 19, the Office Action states that “forming a fourth dielectric layer using a different material from that of the second dielectric layer, on the second dielectric layer” and “removing a portion of the fourth dielectric layer so as to selectively expose a portion of the second dielectric layer”, in claim 19, is new matter.

The specification as filed, at least at page 14, second paragraph, lines 8-13, discloses an embodiment of forming a fourth dielectric layer on a second dielectric layer and etching a portion of the fourth dielectric layer. Specifically, the specification recites at page 14, second paragraph, lines 8-13:

While an example of the gate dielectric layer having three different thicknesses is explained in the second embodiment, it is also possible to embody a gate dielectric layer having more than three thicknesses. That is, additional layers, such as a fourth dielectric layer, formed of other dielectric materials can be sequentially formed on the second dielectric layer 300 presented in the second embodiment and successively etched.

It is therefore submitted that the referenced subject matter of claim 19 is clearly supported by the specification as filed, and therefore is not new matter. Accordingly, reconsideration of the rejection of claim 19 under 35 U.S.C. 112, first paragraph, and allowance of claim 19, are respectfully requested.

Claims 1-4, 6 and 7 stand rejected under 35 U.S.C. 102(a) as being anticipated by Chern, *et al.* (U.S. Publication Number 2003/0102504). Claims 1, 2, 6 and 7 stand rejected under 35 U.S.C. 102(b) as being unpatentable over Kim, *et al.* (U.S. Publication Number 2002/0119615) Claims 5, 8, and 9 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chern, *et al.* Reconsideration of the rejection and allowance of claims 1-9 are respectfully requested.

In the present invention as claimed in independent claim 1, a method of manufacturing a semiconductor device including a multi-thickness gate dielectric layer of a semiconductor device includes forming a first dielectric layer on a semiconductor substrate of a first thickness, forming a second dielectric layer of a second thickness on the top surface of the first dielectric layer, the second dielectric layer having a different dielectric material from that of the first dielectric layer, and further selectively removing a portion of the second dielectric layer with etch selectivity to the first dielectric so as to selectively expose a portion of the top surface of the first dielectric layer under the second dielectric layer to form a gate dielectric layer including a thick portion formed of the first dielectric layer and remaining second dielectric layer and a thin portion formed of the exposed first dielectric layer, the thin portion being of the first thickness and the thick portion being of a combined thickness of the first thickness and the second thickness.

Claim 1 is further amended above to clarify the invention thereby claimed. In particular, claim 1 is amended to state “forming a first transistor in the first region, the first transistor including a first gate dielectric layer comprising a portion of the thick portion of the gate dielectric layer and a second transistor in the second region, the second transistor including a second gate dielectric layer comprising a portion of the thin portion of the gate dielectric layer”. This limitation is clearly supported throughout the specification as filed. For example, this limitation is supported at least at page 9, lines 8-10 and page 9, lines 14-16 of the specification as filed. It is apparent throughout the specification as filed that the “thick portion” and the “thin portion” of the gate dielectric layer are applied to transistors of first and second regions of the resulting device, as gate dielectric layers of the respective transistors. See, for example, page 2, lines 2-5 of the

Background of the Invention section of the specification as filed. Accordingly, it should be clear that the limitation added by amendment above is clearly supported throughout the specification as filed.

As stated in the Amendment D mailed on May 17, 2006, Chern, *et al.*, discloses the formation of a nitride layer 48 on an oxide layer 46 in a semiconductor memory device (see FIG. 3C). The nitride layer 48 is etched in a peripheral area 34 of the device, while the nitride layer 48 in a memory cell area 32 of the device remains intact (see FIG. 3D). A thermal oxidation process is next used to thicken the oxide layer 46 in the peripheral area 34, while the nitride layer 48 in the memory cell area 32 operates as a mask so that the oxide layer 46 thickens only in the peripheral area 34 during the thermal oxidation process (see FIG. 3E). The nitride layer 48 in the cell area 32 is then removed. The resulting oxide layer 46 includes two portions, a thinner portion 72 in the memory cell area 32 and a thicker portion 74 in the peripheral area 34 (see FIG. 3F). The thinner portion 72 and the thicker portion 74 of the oxide layer 46 are both oxide layers, and thus are formed of the same dielectric material.

Chern, *et al.* fails to teach or suggest “forming a gate dielectric layer including a thick portion formed” of a “first dielectric layer and remaining second dielectric layer in a first region of the semiconductor device and a thin portion formed of the exposed first dielectric layer in a second region of the semiconductor device”, the “second dielectric layer having different dielectric material from that of the first dielectric material” and “forming a first transistor in the first region, the first transistor including a first gate dielectric layer comprising a portion of the thick portion of the gate dielectric layer and a second transistor in the second region, the second transistor including a second gate dielectric layer comprising a portion of the thin portion of the gate dielectric layer”, as claimed in claim 1 of the present invention. Instead, in Chern, *et al.*, the nitride layer 48 is used only as an etch mask and is then subsequently fully removed. The nitride layer 48 and the oxide layer 46 of Chern, *et al.* are not included in “a first transistor” of the resulting device and the oxide layer 46 is not included in a “second transistor” of the resulting device, and therefore nitride layer 48 and the oxide layer 46 are not dielectric layers that are used to form the “gate dielectric layer”, that is in turn used in forming the

“first transistor” and the “second transistor” as claimed. The Chern, *et al.* oxide layer 46 is grown in a thermal oxidation process in a peripheral region such that the resulting oxide layer 46 includes a thicker portion 74 and a thinner portion 72. However, the Chern, *et al.* oxide layer 46 in the thicker portion 74 is of the same dielectric material as the oxide layer 46 in the thinner portion 72. Therefore, Chern, *et al.* fails to teach or suggest formation of a “second dielectric layer having different dielectric material from that of” a “first dielectric material”, as claimed in claim 1.

It is therefore submitted that independent claim 1 is allowable over Chern, *et al.* Reconsideration of the rejection of claim 1 under 35 U.S.C. 102(a) as being anticipated by Chern, *et al.*, and allowance of the claim, are respectfully requested. With regard to the rejection of dependent claims 2-4, 6 and 7 as being anticipated by Chern, *et al.* and claims 5, 8 and 9 as being unpatentable over Chern, *et al.*, it follows that these claims should inherit the allowability of the independent claim from which they depend.

As stated in the Amendment D mailed on May 17, 2006, Kim, *et al.* discloses the sequential formation of a pad oxide layer 103, a pad nitride layer 105, and a mask oxide layer 107 on a main surface of a semiconductor substrate 101 (see FIG. 13). A first photoresist layer 109 exposing a first region a of the device is formed on the mask oxide layer 107. The mask oxide layer 107 is etched using the first photoresist pattern 109 as an etching mask to form a patterned mask oxide layer 107a covering a second region b of the device (see FIG. 14). The pad nitride layer 105 is etched in the first region a using the patterned mask oxide layer 107a as an etching mask to form a patterned pad nitride layer 105a covering the second region b (see FIG. 15). The pad oxide layer is then etched using the patterned pad nitride layer 105a as an etching mask to form a patterned pad oxide layer 103a covering the second region b. As a result, the patterned mask oxide layer 107a is removed and the substrate 101 is exposed in the first region a. A thermal oxidation process is applied to the exposed surface of the substrate 101 in the first region a to form a first gate insulating layer 111 in the first region a (see FIG. 16). The patterned pad nitride layer 105a and the patterned pad oxide layer 103a are then etched to expose the substrate 101 in the second region b and the first gate insulating layer 111 is recessed to form first gate insulating layer 111a (see FIG. 17). A thermal oxidation

process is applied to the surface of the substrate 101 in the second region b, forming a second gate insulating layer 113 (see FIG. 18). In the Kim, *et al.* process, the original pad oxide layer 103, the original pad nitride layer 105, and the original mask oxide layer 107 are used only as etch masks, and are completely removed in the eventual formation of the dual-thickness gate insulating layer 111a, 113.

Kim, *et al.* fails to teach or suggest “forming a gate dielectric layer including a thick portion formed” of a “first dielectric layer and remaining second dielectric layer in a first region of the semiconductor device and a thin portion formed of the exposed first dielectric layer in a second region of the semiconductor device”, the “second dielectric layer having different dielectric material from that of the first dielectric material” and “forming a first transistor in the first region, the first transistor including a first gate dielectric layer comprising a portion of the thick portion of the gate dielectric layer and a second transistor in the second region, the second transistor including a second gate dielectric layer comprising a portion of the thin portion of the gate dielectric layer”, as claimed in claim 1 of the present invention. Instead, in Kim, *et al.*, the pad oxide layer 103, the pad nitride layer 105, and the mask oxide layer 107 are used only as etch masks and are then fully removed in the eventual formation of the dual-thickness gate insulating layer 111a, 113. The Kim, *et al.* pad oxide layer 103, pad nitride layer 105, and mask oxide layer 107 are not included in “a first transistor” of the resulting device or a “second transistor” of the resulting device and therefore are not the “dielectric layers” used to form the “gate dielectric layer” that is in turn used in forming the “first transistor” and the “second transistor”, as claimed. In addition, the Kim, *et al.* first gate insulating layer 111a and the second gate insulating layer 113 which are formed in a thicker portion and a thinner portion respectively are formed of the same dielectric material. Therefore, Kim, *et al.* fails to teach or suggest a “second dielectric layer having a different dielectric material from that of” a “first dielectric material”, as claimed in claim 1.

It is therefore submitted that independent claim 1 is allowable over Kim, *et al.* Reconsideration of the rejection of claim 1 under 35 U.S.C. 102(b) as being anticipated by Kim, *et al.*, and allowance of the claim, are respectfully requested. With regard to the rejection of dependent claims 2, 6 and 7 as being anticipated by Kim, *et al.*, it follows

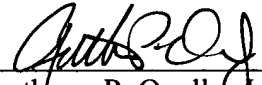
that these claims should inherit the allowability of the independent claim from which they depend.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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